

# UP/DOWN Counter Tables with Pin Labels

This PDF includes the corrected counter-to-decoder table and added pin-label definitions for the main components used in the circuit.

**Table 1: Input Control Table**

UP input	DOWN input	Counter input used	Counter action	Decoder receives	Seven-segment result
0	0	No clock pulse	Holds current value	Same BCD as before	Same number stays displayed
1 pulse	0	UP pin	Counts upward	New BCD value	Display increases by 1
0	1 pulse	DOWN pin	Counts downward	New BCD value	Display decreases by 1
1	1	UP and DOWN together	Not recommended	Unstable / invalid control	Display may be incorrect

**Table 2: Counter -> Decoder -> Seven-Segment Table**

Counter-to-decoder mapping: **Q0 -> A, Q1 -> B, Q2 -> C, Q3 -> D**. The seven-segment column is ordered as **a b c d e f g**, where **1 = ON** and **0 = OFF**.

Counter output (Q3 Q2 Q1 Q0)	Decoder input (D C B A)	Decimal count	Seven-segment display (a b c d e f g)
0000	0000	0	1 1 1 1 1 1 0
0001	0001	1	0 1 1 0 0 0 0
0010	0010	2	1 1 0 1 1 0 1
0011	0011	3	1 1 1 1 0 0 1
0100	0100	4	0 1 1 0 0 1 1
0101	0101	5	1 0 1 1 0 1 1
0110	0110	6	1 0 1 1 1 1 1
0111	0111	7	1 1 1 0 0 0 0
1000	1000	8	1 1 1 1 1 1 1
1001	1001	9	1 1 1 1 0 1 1

**Table 3: Seven-Segment Output Pattern**

For the 74LS48 with a common-cathode display: **1 = segment ON** and **0 = segment OFF**.

Decimal	a	b	c	d	e	f	g	Display
0	1	1	1	1	1	1	0	0
1	0	1	1	0	0	0	0	1
2	1	1	0	1	1	0	1	2
3	1	1	1	1	0	0	1	3
4	0	1	1	0	0	1	1	4
5	1	0	1	1	0	1	1	5
6	1	0	1	1	1	1	1	6
7	1	1	1	0	0	0	0	7
8	1	1	1	1	1	1	1	8
9	1	1	1	1	0	1	1	9

**Table 4: Both Seven-Segment Displays Together**

This table places the upper display and lower display in one place. It shows which counter and decoder/driver controls each display.

Digit position	Counter IC	Counter output (Q3 Q2 Q1 Q0)	Decoder/Driver IC	Decoder input (D C B A)	Display type	Displayed digit	Function
Upper digit	U37 (74LS192)	0000	U38 (74LS48)	0000	Upper common-cathode 7-segment display	0	Receives BCD from U37 through U38 and displays the upper digit.
Lower digit	U39 (74LS192)	0110	U40 (74LS48)	0110	Lower common-cathode 7-segment display	6	Receives BCD from U39 through U40 and displays the lower digit.

**Table 5: Segment States for Both Displays in the Shown Circuit State**

The segment states are listed in the order **a b c d e f g**. A value of **1** means the segment is ON, and **0** means the segment is OFF. In the shown circuit state, the displays read **06**.

Digit position	Displayed digit	BCD input (D C B A)	a	b	c	d	e	f	g	Segment pattern (a b c d e f g)
Upper display	0	0000	1	1	1	1	1	1	0	1 1 1 1 1 1 0
Lower display	6	0110	1	0	1	1	1	1	1	1 0 1 1 1 1 1

## Simple Working Flow

Stage	What happens
UP/DOWN button	Sends a pulse to the counter
74LS192 counter	Produces a 4-bit BCD number
74LS48 decoder	Converts BCD into seven-segment signals
330 Ohm resistors	Limit current to protect the display
Seven-segment display	Shows the decimal number

*UP/DOWN input -> Counter -> Decoder -> Seven-segment display*

## Pin Labels, Meaning, and Definitions

The tables below define the important pin labels used by the components in the circuit. In Proteus, some power pins such as VCC and GND may be hidden, but the ICs still require a 5 V supply and a common 0 V reference.

**Table 6: 74LS08 AND Gate Pin Labels**

Component	Pin label	Meaning	Definition / use in the circuit
U41A / U41B 74LS08	A input	First logic input of an AND gate	Receives one control signal, such as the UP or DOWN button signal.
U41A / U41B 74LS08	B input	Second logic input of an AND gate	Receives the second control or enable signal needed before the clock pulse is passed.
U41A / U41B 74LS08	Y output	AND gate output	Goes HIGH only when both A and B inputs are HIGH. This output is used as the controlled UP or DOWN pulse.
74LS08 IC	VCC	+5 V supply pin	Powers the 74LS08 logic IC.
74LS08 IC	GND	Ground pin	0 V reference for the 74LS08 logic IC.

**Table 7: 74LS192 Up/Down Decade Counter Pin Labels**

Component	Pin label	Meaning	Definition / use in the circuit
U37 / U39 74LS192	D0, D1, D2, D3	Parallel data inputs	Input pins used to load a starting BCD value into the counter when PL is activated. D0 is the least significant input and D3 is the most significant input.
U37 / U39 74LS192	Q0, Q1, Q2, Q3	BCD counter outputs	Four-bit BCD output from the counter. Q0 is the least significant bit and Q3 is the most significant bit.
U37 / U39 74LS192	UP	Count-up clock input	Each valid pulse on this pin increases the BCD count by one.
U37 / U39 74LS192	DN	Count-down clock input	Each valid pulse on this pin decreases the BCD count by one.
U37 / U39 74LS192	PL	Parallel load input	Active-LOW input. When LOW, the counter loads the value present on D0-D3.
U37 / U39 74LS192	MR	Master reset input	Reset input. When activated, the counter output is cleared to 0000.
U37 / U39 74LS192	CU	Carry output	Used for cascading counters during upward counting. It can trigger the next digit when the current digit rolls over.
U37 / U39 74LS192	CD	Borrow output	Used for cascading counters during downward counting. It can trigger the next digit when the current digit rolls under.
74LS192 IC	VCC	+5 V supply pin	Powers the counter IC.
74LS192 IC	GND	Ground pin	0 V reference for the counter IC.

## Pin Labels, Meaning, and Definitions - Continued

**Table 8: 74LS48 BCD-to-Seven-Segment Decoder/Driver Pin Labels**

Component	Pin label	Meaning	Definition / use in the circuit
U38 / U40 74LS48	A, B, C, D	BCD input pins	Receive the 4-bit BCD value from the counter outputs. A receives Q0, B receives Q1, C receives Q2, and D receives Q3.
U38 / U40 74LS48	QA, QB, QC, QD, QE, QF, QG	Seven-segment output pins	Drive the display segments a, b, c, d, e, f, and g through the 330 Ohm resistors.
U38 / U40 74LS48	LT	Lamp test input	Active-LOW test input. When LOW, it turns on all segments for testing. For normal operation it should be kept HIGH.
U38 / U40 74LS48	RBI	Ripple blanking input	Active-LOW blanking input used to remove leading zeros in multi-digit displays. If not used, keep it HIGH.
U38 / U40 74LS48	BI/RBO	Blanking input / ripple blanking output	Active-LOW blanking control. It can blank the display or pass blanking to another decoder in cascaded displays. For normal display, keep it HIGH.
74LS48 IC	VCC	+5 V supply pin	Powers the decoder/driver IC.
74LS48 IC	GND	Ground pin	0 V reference for the decoder/driver IC.

**Table 9: Common-Cathode Seven-Segment Display Pin Labels**

Component	Pin label	Meaning	Definition / use in the circuit
Upper / lower display	a	Top segment	Lights the top horizontal segment of the digit.
Upper / lower display	b	Upper-right segment	Lights the upper-right vertical segment of the digit.
Upper / lower display	c	Lower-right segment	Lights the lower-right vertical segment of the digit.
Upper / lower display	d	Bottom segment	Lights the bottom horizontal segment of the digit.
Upper / lower display	e	Lower-left segment	Lights the lower-left vertical segment of the digit.
Upper / lower display	f	Upper-left segment	Lights the upper-left vertical segment of the digit.
Upper / lower display	g	Middle segment	Lights the middle horizontal segment of the digit.
Upper / lower display	COM / Cathode	Common cathode pin	Common negative terminal for the LED segments. It is connected to GND in a common-cathode display.
Upper / lower display	DP	Decimal point	Optional decimal-point LED. It is not required for the displayed numbers 0-9 in this circuit.

## Other Component Pin / Terminal Definitions

**Table 10: Push Buttons, Reset, Resistors, VCC, and GND**

Component	Pin / terminal label	Meaning	Definition / use in the circuit
UP push button	UP terminal	Count-up input command	When pressed, it creates a pulse that is passed through the control logic to the UP clock input of the 74LS192 counter.
DOWN push button	DOWN terminal	Count-down input command	When pressed, it creates a pulse that is passed through the control logic to the DN clock input of the 74LS192 counter.
RESET push button	RESET terminal	Clear/reset command	When pressed, it activates the reset line so the counter returns to 0000.
Pull resistor	R149	Bias / pull resistor	Provides a stable logic level so the input does not float when the push button is not pressed.
Segment resistors	R134 / R142	Current-limiting resistors	Each 330 Ohm resistor is connected in series between a decoder output and a seven-segment display LED segment.
VCC symbol	VCC	Positive supply rail	Provides the +5 V logic supply required by the 74LS-series ICs.
Ground symbol	GND	0 V reference rail	Common reference point for the circuit and the return path for the common-cathode displays.

### Important connection summary

Connection	Meaning
Counter Q0 -> Decoder A	Least significant BCD bit goes to the decoder A input.
Counter Q1 -> Decoder B	Second BCD bit goes to the decoder B input.
Counter Q2 -> Decoder C	Third BCD bit goes to the decoder C input.
Counter Q3 -> Decoder D	Most significant BCD bit goes to the decoder D input.
Decoder QA-QG -> 330 Ohm -> Display a-g	Decoder outputs pass through current-limiting resistors before driving the display segments.

# Counting from 00 to 99

This section adds the full two-digit counting table for the circuit. The upper counter/display represents the tens digit, and the lower counter/display represents the ones digit. For the seven-segment columns, the states are written in the order **a b c d e f g**, where **1 = segment ON** and **0 = segment OFF**.

Part	Role in 00-99 counting
U39 lower counter (74LS192)	Counts the ones digit from 0 to 9 for each UP pulse.
U40 lower decoder (74LS48)	Converts the U39 BCD output into seven-segment signals for the lower display.
U37 upper counter (74LS192)	Counts the tens digit. It changes when the lower counter rolls over from 9 to 0, or borrows when counting down.
U38 upper decoder (74LS48)	Converts the U37 BCD output into seven-segment signals for the upper display.
Two displays together	Show the complete number from 00 to 99.

**Table 6: Full Two-Digit Count from 00 to 99**

Count	Upper counter output U37 Q3 Q2 Q1 Q0	Upper decoder input U38 D C B A	Upper display segments a b c d e f g	Lower counter output U39 Q3 Q2 Q1 Q0	Lower decoder input U40 D C B A	Lower display segments a b c d e f g	Displayed number
00	0000	0000	1 1 1 1 1 1 0	0000	0000	1 1 1 1 1 1 0	00
01	0000	0000	1 1 1 1 1 1 0	0001	0001	0 1 1 0 0 0 0	01
02	0000	0000	1 1 1 1 1 1 0	0010	0010	1 1 0 1 1 0 1	02
03	0000	0000	1 1 1 1 1 1 0	0011	0011	1 1 1 1 0 0 1	03
04	0000	0000	1 1 1 1 1 1 0	0100	0100	0 1 1 0 0 1 1	04
05	0000	0000	1 1 1 1 1 1 0	0101	0101	1 0 1 1 0 1 1	05
06	0000	0000	1 1 1 1 1 1 0	0110	0110	1 0 1 1 1 1 1	06
07	0000	0000	1 1 1 1 1 1 0	0111	0111	1 1 1 0 0 0 0	07
08	0000	0000	1 1 1 1 1 1 0	1000	1000	1 1 1 1 1 1 1	08
09	0000	0000	1 1 1 1 1 1 0	1001	1001	1 1 1 1 0 1 1	09
10	0001	0001	0 1 1 0 0 0 0	0000	0000	1 1 1 1 1 1 0	10
11	0001	0001	0 1 1 0 0 0 0	0001	0001	0 1 1 0 0 0 0	11
12	0001	0001	0 1 1 0 0 0 0	0010	0010	1 1 0 1 1 0 1	12
13	0001	0001	0 1 1 0 0 0 0	0011	0011	1 1 1 1 0 0 1	13
14	0001	0001	0 1 1 0 0 0 0	0100	0100	0 1 1 0 0 1 1	14
15	0001	0001	0 1 1 0 0 0 0	0101	0101	1 0 1 1 0 1 1	15
16	0001	0001	0 1 1 0 0 0 0	0110	0110	1 0 1 1 1 1 1	16
17	0001	0001	0 1 1 0 0 0 0	0111	0111	1 1 1 0 0 0 0	17
18	0001	0001	0 1 1 0 0 0 0	1000	1000	1 1 1 1 1 1 1	18
19	0001	0001	0 1 1 0 0 0 0	1001	1001	1 1 1 1 0 1 1	19
20	0010	0010	1 1 0 1 1 0 1	0000	0000	1 1 1 1 1 1 0	20
21	0010	0010	1 1 0 1 1 0 1	0001	0001	0 1 1 0 0 0 0	21
22	0010	0010	1 1 0 1 1 0 1	0010	0010	1 1 0 1 1 0 1	22
23	0010	0010	1 1 0 1 1 0 1	0011	0011	1 1 1 1 0 0 1	23
24	0010	0010	1 1 0 1 1 0 1	0100	0100	0 1 1 0 0 1 1	24
25	0010	0010	1 1 0 1 1 0 1	0101	0101	1 0 1 1 0 1 1	25

Count	Upper counter output U37 Q3 Q2 Q1 Q0	Upper decoder input U38 D C B A	Upper display segments a b c d e f g	Lower counter output U39 Q3 Q2 Q1 Q0	Lower decoder input U40 D C B A	Lower display segments a b c d e f g	Displayed number
26	0010	0010	1 1 0 1 1 0 1	0110	0110	1 0 1 1 1 1 1	26
27	0010	0010	1 1 0 1 1 0 1	0111	0111	1 1 1 0 0 0 0	27
28	0010	0010	1 1 0 1 1 0 1	1000	1000	1 1 1 1 1 1 1	28
29	0010	0010	1 1 0 1 1 0 1	1001	1001	1 1 1 1 0 1 1	29
30	0011	0011	1 1 1 1 0 0 1	0000	0000	1 1 1 1 1 1 0	30
31	0011	0011	1 1 1 1 0 0 1	0001	0001	0 1 1 0 0 0 0	31
32	0011	0011	1 1 1 1 0 0 1	0010	0010	1 1 0 1 1 0 1	32
33	0011	0011	1 1 1 1 0 0 1	0011	0011	1 1 1 1 0 0 1	33
34	0011	0011	1 1 1 1 0 0 1	0100	0100	0 1 1 0 0 1 1	34
35	0011	0011	1 1 1 1 0 0 1	0101	0101	1 0 1 1 0 1 1	35
36	0011	0011	1 1 1 1 0 0 1	0110	0110	1 0 1 1 1 1 1	36
37	0011	0011	1 1 1 1 0 0 1	0111	0111	1 1 1 0 0 0 0	37
38	0011	0011	1 1 1 1 0 0 1	1000	1000	1 1 1 1 1 1 1	38
39	0011	0011	1 1 1 1 0 0 1	1001	1001	1 1 1 1 0 1 1	39
40	0100	0100	0 1 1 0 0 1 1	0000	0000	1 1 1 1 1 1 0	40
41	0100	0100	0 1 1 0 0 1 1	0001	0001	0 1 1 0 0 0 0	41
42	0100	0100	0 1 1 0 0 1 1	0010	0010	1 1 0 1 1 0 1	42
43	0100	0100	0 1 1 0 0 1 1	0011	0011	1 1 1 1 0 0 1	43
44	0100	0100	0 1 1 0 0 1 1	0100	0100	0 1 1 0 0 1 1	44
45	0100	0100	0 1 1 0 0 1 1	0101	0101	1 0 1 1 0 1 1	45
46	0100	0100	0 1 1 0 0 1 1	0110	0110	1 0 1 1 1 1 1	46
47	0100	0100	0 1 1 0 0 1 1	0111	0111	1 1 1 0 0 0 0	47
48	0100	0100	0 1 1 0 0 1 1	1000	1000	1 1 1 1 1 1 1	48
49	0100	0100	0 1 1 0 0 1 1	1001	1001	1 1 1 1 0 1 1	49
50	0101	0101	1 0 1 1 0 1 1	0000	0000	1 1 1 1 1 1 0	50
51	0101	0101	1 0 1 1 0 1 1	0001	0001	0 1 1 0 0 0 0	51
52	0101	0101	1 0 1 1 0 1 1	0010	0010	1 1 0 1 1 0 1	52
53	0101	0101	1 0 1 1 0 1 1	0011	0011	1 1 1 1 0 0 1	53
54	0101	0101	1 0 1 1 0 1 1	0100	0100	0 1 1 0 0 1 1	54
55	0101	0101	1 0 1 1 0 1 1	0101	0101	1 0 1 1 0 1 1	55
56	0101	0101	1 0 1 1 0 1 1	0110	0110	1 0 1 1 1 1 1	56
57	0101	0101	1 0 1 1 0 1 1	0111	0111	1 1 1 0 0 0 0	57
58	0101	0101	1 0 1 1 0 1 1	1000	1000	1 1 1 1 1 1 1	58
59	0101	0101	1 0 1 1 0 1 1	1001	1001	1 1 1 1 0 1 1	59
60	0110	0110	1 0 1 1 1 1 1	0000	0000	1 1 1 1 1 1 0	60
61	0110	0110	1 0 1 1 1 1 1	0001	0001	0 1 1 0 0 0 0	61
62	0110	0110	1 0 1 1 1 1 1	0010	0010	1 1 0 1 1 0 1	62
63	0110	0110	1 0 1 1 1 1 1	0011	0011	1 1 1 1 0 0 1	63
64	0110	0110	1 0 1 1 1 1 1	0100	0100	0 1 1 0 0 1 1	64
65	0110	0110	1 0 1 1 1 1 1	0101	0101	1 0 1 1 0 1 1	65
66	0110	0110	1 0 1 1 1 1 1	0110	0110	1 0 1 1 1 1 1	66
67	0110	0110	1 0 1 1 1 1 1	0111	0111	1 1 1 0 0 0 0	67



Count	Upper counter output U37 Q3 Q2 Q1 Q0	Upper decoder input U38 D C B A	Upper display segments a b c d e f g	Lower counter output U39 Q3 Q2 Q1 Q0	Lower decoder input U40 D C B A	Lower display segments a b c d e f g	Displayed number
68	0110	0110	1 0 1 1 1 1 1	1000	1000	1 1 1 1 1 1 1	68
69	0110	0110	1 0 1 1 1 1 1	1001	1001	1 1 1 1 0 1 1	69
70	0111	0111	1 1 1 0 0 0 0	0000	0000	1 1 1 1 1 1 0	70
71	0111	0111	1 1 1 0 0 0 0	0001	0001	0 1 1 0 0 0 0	71
72	0111	0111	1 1 1 0 0 0 0	0010	0010	1 1 0 1 1 0 1	72
73	0111	0111	1 1 1 0 0 0 0	0011	0011	1 1 1 1 0 0 1	73
74	0111	0111	1 1 1 0 0 0 0	0100	0100	0 1 1 0 0 1 1	74
75	0111	0111	1 1 1 0 0 0 0	0101	0101	1 0 1 1 0 1 1	75
76	0111	0111	1 1 1 0 0 0 0	0110	0110	1 0 1 1 1 1 1	76
77	0111	0111	1 1 1 0 0 0 0	0111	0111	1 1 1 0 0 0 0	77
78	0111	0111	1 1 1 0 0 0 0	1000	1000	1 1 1 1 1 1 1	78
79	0111	0111	1 1 1 0 0 0 0	1001	1001	1 1 1 1 0 1 1	79
80	1000	1000	1 1 1 1 1 1 1	0000	0000	1 1 1 1 1 1 0	80
81	1000	1000	1 1 1 1 1 1 1	0001	0001	0 1 1 0 0 0 0	81
82	1000	1000	1 1 1 1 1 1 1	0010	0010	1 1 0 1 1 0 1	82
83	1000	1000	1 1 1 1 1 1 1	0011	0011	1 1 1 1 0 0 1	83
84	1000	1000	1 1 1 1 1 1 1	0100	0100	0 1 1 0 0 1 1	84
85	1000	1000	1 1 1 1 1 1 1	0101	0101	1 0 1 1 0 1 1	85
86	1000	1000	1 1 1 1 1 1 1	0110	0110	1 0 1 1 1 1 1	86
87	1000	1000	1 1 1 1 1 1 1	0111	0111	1 1 1 0 0 0 0	87
88	1000	1000	1 1 1 1 1 1 1	1000	1000	1 1 1 1 1 1 1	88
89	1000	1000	1 1 1 1 1 1 1	1001	1001	1 1 1 1 0 1 1	89
90	1001	1001	1 1 1 1 0 1 1	0000	0000	1 1 1 1 1 1 0	90
91	1001	1001	1 1 1 1 0 1 1	0001	0001	0 1 1 0 0 0 0	91
92	1001	1001	1 1 1 1 0 1 1	0010	0010	1 1 0 1 1 0 1	92
93	1001	1001	1 1 1 1 0 1 1	0011	0011	1 1 1 1 0 0 1	93
94	1001	1001	1 1 1 1 0 1 1	0100	0100	0 1 1 0 0 1 1	94
95	1001	1001	1 1 1 1 0 1 1	0101	0101	1 0 1 1 0 1 1	95
96	1001	1001	1 1 1 1 0 1 1	0110	0110	1 0 1 1 1 1 1	96
97	1001	1001	1 1 1 1 0 1 1	0111	0111	1 1 1 0 0 0 0	97
98	1001	1001	1 1 1 1 0 1 1	1000	1000	1 1 1 1 1 1 1	98
99	1001	1001	1 1 1 1 0 1 1	1001	1001	1 1 1 1 0 1 1	99

*UP count sequence: 00, 01, 02, ... 09, 10, 11, ... 99. DOWN count sequence: 99, 98, 97, ... 00.*

# LED Control Tables for the 00-99 Digital Counter

These tables explain why the tens counter outputs A and B were used to control the green, yellow, and red flashing LED ranges. The LED colour depends on the tens digit only, not the ones digit.

**Table 6: Tens counter output selection for LED ranges**

The counter display goes from 00 to 99. For the LED indicator, only the tens digit is checked. Therefore, the circuit uses the tens counter bits A and B, where A = Q0 and B = Q1.

Full count range	Tens digit	Tens counter BCD (Q3 Q2 Q1 Q0)	A = Q0	B = Q1	Required LED	Reason
00-09	0	0000	0	0	Green LED	Tens digit is 0 for all numbers from 00 to 09.
10-19	1	0001	1	0	Yellow LED	Tens digit is 1 for all numbers from 10 to 19.
20-29	2	0010	0	1	Red flashing LED	Tens digit is 2 for all numbers from 20 to 29.
30-39	3	0011	1	1	Not selected	This condition is not part of the three LED ranges unless extra logic is added.

**Table 7: LED Boolean logic using tens counter pins A and B**

The inverter gates produce /A and /B. The AND gates then select only one LED range at a time.

A	B	/A	/B	Selected decimal range	Logic expression	LED output	Output behaviour
0	0	1	1	00-09	NOT A AND NOT B	Green LED ON	Normal/safe range. Green LED stays ON continuously.
1	0	0	1	10-19	A AND NOT B	Yellow LED ON	Warning range. Yellow LED stays ON continuously.
0	1	1	0	20-29	NOT A AND B	Red flashing LED ON	Danger/high range. The AND output enables the relay/NE555 flashing circuit.
1	1	0	0	30-39	A AND B	No LED in this design	This range is not selected by the shown three LED outputs.

**Table 8: LED control gates and component assignment**

Range detected	Tens condition	Logic used	AND gate/output path	Indicator component	Meaning
00-09	A = 0, B = 0	NOT A AND NOT B	U4 output	D2 Green LED through R2	The count is from 00 to 09; the green LED shows the low/safe range.
10-19	A = 1, B = 0	A AND NOT B	U8 output	D4 Yellow LED through R4	The count is from 10 to 19; the yellow LED shows the middle/warning range.
20-29	A = 0, B = 1	NOT A AND B	U7 output	Relay RL1 and NE555 flashing red LEDs D7/D8	The count is from 20 to 29; the red LEDs flash to show the high/danger range.

**Important note:** In the shown logic, the label should be **20-29**, not 20-30. At 30, the tens digit is 3, so A = 1 and B = 1. That would require an additional **A AND B** logic path if 30 must also activate the red warning.

# Pin and Component Meaning for the LED Control Interface

The following tables define the labels and components used in the LED control section connected to the tens counter.

**Table 9: Signal labels used by the LED control interface**

Label	Source	Meaning	Definition / use in this circuit
A	Tens counter Q0	Least significant bit of the tens digit	Used to distinguish tens digit 0, 1, 2, and 3 when combined with B.
B	Tens counter Q1	Second bit of the tens digit	Used with A to detect the selected ranges 00-09, 10-19, and 20-29.
/A	Output of inverter gate	Inverted A signal	Becomes 1 when A = 0. Used for green and red range detection.
/B	Output of inverter gate	Inverted B signal	Becomes 1 when B = 0. Used for green and yellow range detection.
00	AND output for green range	Logic output for A = 0 and B = 0	Turns ON the green LED for 00-09.
10	AND output for yellow/red logic	Logic output for the selected range	Depending on the gate path, it indicates either 10-19 for yellow or 20-29 for red flashing.

**Table 10: Component meaning in the LED control section**

Component	Type / label	Purpose	Definition in the circuit
U5, U6, U10, U9	Inverter gates	Generate /A and /B	They change a logic 1 into 0 and a logic 0 into 1 so the AND gates can detect ranges such as 00-09.
U4, U7, U8	2-input AND gates	Range detection	Each AND gate outputs 1 only when its two required input conditions are both true.
D2	Green LED	Low-range indicator	ON when the count is 00-09.
D4	Yellow LED	Mid-range indicator	ON when the count is 10-19.
RL1	5 V relay	Switch/enable flashing stage	Activated by the red-range logic to connect power/control to the NE555 flashing circuit.
U2	NE555 timer	Flashing red LED control	Works as an oscillator/astable timing circuit to make D7 and D8 flash.
D7, D8	Red LEDs	High-range warning	Flash when the count is in the 20-29 range.
R2, R4, R9, R10	Current-limiting resistors	Protect LEDs	Limit current so the LEDs are not damaged.
R8 and C2	Timing network	Set flashing rate	Together with the NE555, they control how fast the red LEDs flash.

*Summary: The ones counter changes from 0 to 9 inside each range, but the LED colour stays the same because only the tens counter pins A and B are used for range detection.*

## Example Counts and LED Status

**Table 11: Example counts and LED status**

Example count	Tens digit	Ones digit	A	B	LED status
00	0	0	0	0	Green ON
05	0	5	0	0	Green ON
09	0	9	0	0	Green ON
10	1	0	1	0	Yellow ON
15	1	5	1	0	Yellow ON
19	1	9	1	0	Yellow ON
20	2	0	0	1	Red flashing
25	2	5	0	1	Red flashing
29	2	9	0	1	Red flashing
30	3	0	1	1	Not selected by current logic

# Complete Pin Labels, Meanings and Definitions

This section explains the pin labels used by the full counter circuit, the LED control interface, and the flashing LED stage. It focuses on what each pin does in this project, so the circuit can be explained during presentation.

**Table 10: 74LS192 Up/Down Decade Counter Pin Meaning**

Component / IC	Pin label	Type	Meaning	Definition / purpose in this circuit
74LS192 counter U32 = tens U34 = ones	D0, D1, D2, D3	Inputs	Parallel data inputs	These inputs are used only when the parallel-load input is activated. They can force a preset BCD value into the counter. In this circuit they are normally tied low, so the counter starts or loads from 0000.
74LS192 counter	Q0, Q1, Q2, Q3	Outputs	BCD output bits	These four outputs carry the BCD number produced by the counter. Q0 is the least significant bit and Q3 is the most significant bit. They feed the 74LS48 decoder.
74LS192 counter	UP	Clock input	Up-count clock	Each valid pulse on this pin increases the count by one. For the ones counter, this advances 0 to 9.
74LS192 counter	DN	Clock input	Down-count clock	Each valid pulse on this pin decreases the count by one.
74LS192 counter	PL	Control input	Parallel load	Active-low load input. When LOW, the counter loads the value present on D0-D3 instead of counting.
74LS192 counter	MR	Control input	Master reset	Reset input. It clears the counter to 0000 when activated. It is used with the reset push-button.
74LS192 counter	TCU	Output	Terminal count up / carry	Used for cascading counters. When the ones digit rolls over upward from 9 to 0, this output helps pulse the tens counter upward.
74LS192 counter	TCD	Output	Terminal count down / borrow	Used for cascading counters. When the ones digit rolls down from 0 to 9, this output helps pulse the tens counter downward.
74LS192 counter	VCC	Power	+5 V supply	Positive supply pin for the TTL IC.
74LS192 counter	GND	Power	0 V reference	Ground reference for the IC and the circuit.

**Table 11: 74LS48 BCD-to-7-Segment Decoder/Driver Pin Meaning**

Component / IC	Pin label	Type	Meaning	Definition / purpose in this circuit
74LS48 decoder / driver U33 = tens U35 = ones	A, B, C, D	Inputs	BCD inputs	These receive the 4-bit BCD value from the 74LS192 counter. A receives Q0, B receives Q1, C receives Q2, and D receives Q3.
74LS48 decoder / driver	QA, QB, QC, QD, QE, QF, QG	Outputs	Segment outputs	These drive the seven display segments a, b, c, d, e, f, and g through 330 ohm resistors. They decide which bars light up for each decimal digit.
74LS48 decoder / driver	LT	Control input	Lamp test	Active-low test input. When activated, it turns on all segments to check whether the display works. It is normally kept inactive in this circuit.
74LS48 decoder / driver	RBI	Control input	Ripple blanking input	Blanking input used to suppress leading zeros in some counter systems. In this project, the display is kept visible, so it is normally inactive.
74LS48 decoder / driver	BI/RBO	Control input / output	Blanking input / ripple blanking output	Can blank the display or pass blanking to the next digit. In this project it is not used for blanking the required 00-99 display.
74LS48 decoder / driver	VCC	Power	+5 V supply	Positive supply pin for the decoder IC.
74LS48 decoder / driver	GND	Power	0 V reference	Ground reference for the decoder IC.

**Table 12: Seven-Segment Display and Segment Resistor Pin Meaning**

Component	Pin / label	Type	Meaning	Definition / purpose in this circuit
Common-cathode 7-segment display	a	LED segment input	Top horizontal segment	Turns on the top bar of the digit.
Common-cathode 7-segment display	b	LED segment input	Upper-right segment	Turns on the upper-right vertical bar.
Common-cathode 7-segment display	c	LED segment input	Lower-right segment	Turns on the lower-right vertical bar.
Common-cathode 7-segment display	d	LED segment input	Bottom horizontal segment	Turns on the bottom bar.
Common-cathode 7-segment display	e	LED segment input	Lower-left segment	Turns on the lower-left vertical bar.
Common-cathode 7-segment display	f	LED segment input	Upper-left segment	Turns on the upper-left vertical bar.
Common-cathode 7-segment display	g	LED segment input	Middle horizontal segment	Turns on the middle bar.
Common-cathode 7-segment display	COM / Cathode	Common terminal	Shared negative terminal	Connected to ground. A segment lights when its corresponding decoder output drives current through the resistor into that segment.
Resistor pack / individual resistors R120, R127	330 ohm	Current limiter	Segment protection	Limits current flowing through each seven-segment LED segment to prevent damage.

# Complete Pin Labels, Meanings and Definitions - Control and LED Interface

**Table 13: 74LS08 AND Gate Pin Meaning**

Component / IC	Pin / label	Type	Meaning	Definition / purpose in this circuit
74LS08 AND gate U36, U4, U7, U8	A input	Logic input	First AND input	One of the two logic conditions entering an AND gate. The output becomes 1 only when both inputs are 1.
74LS08 AND gate	B input	Logic input	Second AND input	The second logic condition entering the AND gate.
74LS08 AND gate	Y / output	Logic output	AND result	Produces the combined condition. In the counter section it passes UP or DOWN pulses. In the LED interface it detects selected tens ranges.
74LS08 AND gate	U36:A, U36:B	Gate sections	Counter input control gates	These gates help form valid UP and DOWN counter pulses.
74LS08 AND gate	U4	Gate section	Green range detector	Detects tens digit 0 using /A AND /B, giving the 00-09 range.
74LS08 AND gate	U8	Gate section	Yellow range detector	Detects tens digit 1 using A AND /B, giving the 10-19 range.
74LS08 AND gate	U7	Gate section	Red flashing range detector	Detects tens digit 2 using /A AND B, giving the 20-29 range and enabling the flashing stage.
74LS08 AND gate	VCC / GND	Power pins	+5 V and 0 V	Supply and ground for the TTL logic IC.

**Table 14: Inverter Pin Meaning Used by the LED Range Logic**

Component / IC	Pin / label	Type	Meaning	Definition / purpose in this circuit
Inverter gates U5, U6, U9, U10	A or B input	Logic input	Original tens bit	Receives the tens counter logic bit. In this project, A = Q0 and B = Q1 from the tens counter.
Inverter gates	/A or /B output	Logic output	Inverted tens bit	Produces the opposite logic level. If A = 1, then /A = 0. If A = 0, then /A = 1.
Inverter gates	U10 and U9	Gate sections	/A and /B for 00-09	Their outputs feed the green LED range detector: /A AND /B.
Inverter gates	U6	Gate section	/B for 10-19	Its output combines with A in the yellow LED detector: A AND /B.
Inverter gates	U5	Gate section	/A for 20-29	Its output combines with B in the red flashing detector: /A AND B.
Inverter gates	VCC / GND	Power pins	+5 V and 0 V	Supply and ground for the TTL inverter IC.

**Table 15: Tens-Counter A/B Signal Labels Used for LED Range Selection**

Signal label	Source pin	Binary meaning	Definition / purpose	Used for
A	Tens counter Q0	Least significant bit of tens digit	A identifies whether the tens digit has bit 0 set. It is used because tens values 0, 1, and 2 can be separated using only A and B.	LED colour selection
B	Tens counter Q1	Second bit of tens digit	B identifies whether the tens digit has bit 1 set. It separates 20-29 from 00-19.	LED colour selection
/A	Inverter output from A	NOT A	Opposite of A. It becomes 1 when A is 0.	Used in green and red conditions
/B	Inverter output from B	NOT B	Opposite of B. It becomes 1 when B is 0.	Used in green and yellow conditions
00	/A AND /B	A=0, B=0	Detects tens digit 0.	Green LED ON for 00-09
10	A AND /B	A=1, B=0	Detects tens digit 1.	Yellow LED ON for 10-19

Signal label	Source pin	Binary meaning	Definition / purpose	Used for
I0	/A AND B	A=0, B=1	Detects tens digit 2.	Enables flashing red LED for 20-29

**Table 16: NE555 Timer Pin Meaning for the Flashing Red LED Stage**

Component / IC	Pin label	Type	Meaning	Definition / purpose in this circuit
NE555 timer U2	1 - GND	Power	Ground	0 V reference for the timer.
NE555 timer	2 - TR	Input	Trigger	Starts the timing cycle when the voltage falls below the trigger level. It is part of the flashing oscillator network.
NE555 timer	3 - Q / OUT	Output	Timer output	Produces the square-wave signal that switches the red LEDs on and off to create the flashing effect.
NE555 timer	4 - R / RESET	Control input	Reset	Active-low reset pin. Kept high when flashing must be allowed; pulling it low stops the timer.
NE555 timer	5 - CV	Control input	Control voltage	Allows adjustment of internal thresholds. Usually left unused or decoupled.
NE555 timer	6 - TH	Input	Threshold	Monitors capacitor voltage and resets the output when the threshold level is reached.
NE555 timer	7 - DC	Output transistor	Discharge	Discharges the timing capacitor through the resistor network to create oscillation.
NE555 timer	8 - VCC	Power	+5 V supply	Positive supply pin for the timer.



# Complete Pin Labels, Meanings and Definitions - Other Components

**Table 17: LED, Resistor and Capacitor Pin / Label Meaning**

Component	Pin / label	Type	Meaning	Definition / purpose in this circuit
D2 - Green LED	Anode	LED positive side	Current enters LED	Lights when the 00-09 condition is true through the green LED logic path.
D2 - Green LED	Cathode	LED negative side	Current leaves LED	Connected toward ground through the circuit return path.
D4 - Yellow LED	Anode	LED positive side	Current enters LED	Lights when the 10-19 condition is true.
D4 - Yellow LED	Cathode	LED negative side	Current leaves LED	Connected toward ground through the circuit return path.
D7 and D8 - Red LEDs	Anode / Cathode	LED terminals	Flashing warning LEDs	Driven by the NE555 output stage so the red LEDs flash during the 20-29 range.
R2, R4	330 ohm	Series resistor	LED current limiter	Limits current through the green and yellow LEDs.
R9, R10	220 ohm	Series resistor	Red LED current limiter	Limits current through the red flashing LEDs.
R8	22 kohm	Timing resistor	555 timing resistor	Works with C2 and the 555 discharge/threshold pins to set the flashing rate.
C2	20 uF	Timing capacitor	555 timing capacitor	Charges and discharges during timer operation; together with R8 it controls the flash speed.

**Table 18: Relay and Switch Pin / Label Meaning**

Component	Pin / label	Type	Meaning	Definition / purpose in this circuit
RL1 - 5 V relay	Coil terminals	Electromagnetic input	Relay coil	When energised, the coil changes the relay contact position. It is used as an interface/isolation element for the flashing LED control path.
RL1 - 5 V relay	COM	Contact	Common contact	The moving contact of the relay switch.
RL1 - 5 V relay	NO	Contact	Normally open contact	Open when the coil is off; closes when the coil is energised.
RL1 - 5 V relay	NC	Contact	Normally closed contact	Closed when the coil is off; opens when the coil is energised. Use depends on the relay wiring selected in the schematic.
UP push button	Input terminal	Manual input	Up-count pulse	Sends a pulse to the UP logic/counter input so the displayed number increases.
DOWN push button	Input terminal	Manual input	Down-count pulse	Sends a pulse to the DOWN logic/counter input so the displayed number decreases.
RESET push button	Reset line	Manual control	Counter reset	Activates the reset path so the counters return to 00.
R137 / pull resistor	330 ohm	Pull/current path	Reference path	Provides a defined circuit path around the reset/input section, depending on the exact wiring in the schematic.

**Table 19: Why Only Tens Counter A and B Are Used**

Tens digit range	Tens BCD (Q3 Q2 Q1 Q0)	A=Q0	B=Q1	Logic condition	Output / action
00-09	0000	0	0	/A AND /B	Green LED ON
10-19	0001	1	0	A AND /B	Yellow LED ON
20-29	0010	0	1	/A AND B	Red LEDs flash using NE555
30-39	0011	1	1	A AND B	Not selected by the shown three LED conditions

# Physical Pin Number Reference for the Main ICs

These pin numbers are for the common DIP versions of the ICs used in the circuit. For the seven-segment display, physical pin numbers can change between display models, so the safest labels are the segment names a, b, c, d, e, f, g and common cathode.

**Table 20: 74LS192 and 74LS48 Physical Pin Number Reference**

IC / component	Physical pin number	Pin label	Meaning	Definition / use
74LS192	15, 1, 10, 9	D0, D1, D2, D3	Parallel data inputs	Preset/load inputs for the counter.
74LS192	3, 2, 6, 7	Q0, Q1, Q2, Q3	BCD outputs	Output bits sent to the 74LS48 decoder.
74LS192	5	UP	Up clock	Pulse input that increases the count.
74LS192	4	DN	Down clock	Pulse input that decreases the count.
74LS192	11	PL	Parallel load	Active-low load control.
74LS192	14	MR	Master reset	Clears the counter to 0000.
74LS192	12	TCU	Carry output	Used to cascade the ones counter into the tens counter when counting up.
74LS192	13	TCD	Borrow output	Used to cascade the ones counter into the tens counter when counting down.
74LS192	16 / 8	VCC / GND	Power pins	+5 V supply and 0 V ground.
74LS48	7, 1, 2, 6	A, B, C, D	BCD inputs	Receives Q0, Q1, Q2, Q3 from the counter.
74LS48	13, 12, 11, 10, 9, 15, 14	QA, QB, QC, QD, QE, QF, QG	Segment outputs	Drive seven-segment display segments a-g through resistors.
74LS48	3	LT	Lamp test	Active-low test input for turning all segments on.
74LS48	5	RBI	Ripple blanking input	Used for leading-zero blanking when required.
74LS48	4	BI/RBO	Blanking input / output	Can blank the display or pass blanking to another digit.
74LS48	16 / 8	VCC / GND	Power pins	+5 V supply and 0 V ground.

**Table 21: Logic Gate, Inverter and NE555 Physical Pin Number Reference**

IC / component	Physical pin number	Pin label	Meaning	Definition / use
74LS08 AND gate	1, 2 -> 3	Gate 1 A, B -> Y	AND gate 1	Output is 1 only when both inputs are 1.
74LS08 AND gate	4, 5 -> 6	Gate 2 A, B -> Y	AND gate 2	Same AND function.
74LS08 AND gate	9, 10 -> 8	Gate 3 A, B -> Y	AND gate 3	Same AND function.
74LS08 AND gate	12, 13 -> 11	Gate 4 A, B -> Y	AND gate 4	Same AND function.
74LS08 AND gate	14 / 7	VCC / GND	Power pins	+5 V supply and 0 V ground.
74LS04 inverter	1 -> 2	Input -> output	Inverter 1	Output is NOT input.
74LS04 inverter	3 -> 4	Input -> output	Inverter 2	Output is NOT input.
74LS04 inverter	5 -> 6	Input -> output	Inverter 3	Output is NOT input.
74LS04 inverter	9 -> 8	Input -> output	Inverter 4	Output is NOT input.
74LS04 inverter	11 -> 10	Input -> output	Inverter 5	Output is NOT input.

IC / component	Physical pin number	Pin label	Meaning	Definition / use
74LS04 inverter	13 -> 12	Input -> output	Inverter 6	Output is NOT input.
74LS04 inverter	14 / 7	VCC / GND	Power pins	+5 V supply and 0 V ground.
NE555 timer	1, 2, 3, 4	GND, TR, OUT, RESET	Timer lower pins	Ground, trigger input, output, and active-low reset.
NE555 timer	5, 6, 7, 8	CV, TH, DC, VCC	Timer upper pins	Control voltage, threshold, discharge, and +5 V supply.